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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,582	02/16/2001	John Susantha Fernando	9-11-4	8752

7590 06/16/2004

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EXAMINER	
CHANDRASEKHAR, PRANAV	
ART UNIT	**PAPER NUMBER**
2115	7

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,582	FERNANDO ET AL.	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/25/2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1,6,8 and 14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Gulick [US Pat No. 6,601,178].

2. As per claim 1, Gulick teaches

adjusting a voltage level of said control signal from a previous time interval to indicate a first signal state [col. 10 lines 19-26. The adjustment of voltage level is indicative of a change in power consumption state]; and

maintaining said voltage level of said control signal from the previous time interval to indicate a second signal state [col. 10 lines 19-26. The maintaining of voltage level is indicative of remaining in the current power consumption state].

3. As per claim 8, Gulick teaches

detecting a first signal state for said control signal if a voltage level from a previous time interval is adjusted [col. 10 lines 19-26. The adjustment of voltage level is indicative of a change in power consumption state]; and

detecting a second signal state if said voltage level from the previous time interval is maintained [col. 10 lines 19-26. The maintaining of voltage level is indicative of remaining in the current power consumption state.].

4. As per claims 6 and 14, Gulick teaches the adjusting step further comprising the step of transitioning from a first voltage level to a second voltage level [col. 10 lines 19-26].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2,7,11,15-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick [US Pat No. 6,601,178] in view of Kanuma [US Pat No. 4,587,445].

6. As per claim 16, Gulick teaches

an adjustment circuit for changing said voltage level from the previous time interval indicating an assertion of said control signal by another device [col. 10 lines 19-26; col. 9 lines 43-48; col. 10 lines 12-14. The change in voltage level is viewed as being facilitated by an adjustment circuit.]

Gulick does not explicitly teach

a memory element for maintaining a voltage level from a previous time interval; and

a comparison circuit for detecting a change in said voltage level from the previous time interval indicating an assertion of said control signal by another device.

Kanuma teaches

a memory element for maintaining a voltage level from a previous time interval [22-1 –22-N Fig 2; col. 3 liens 33-61; col. 4 lines 15-20. Based on the cited lines, it is evident that a D flip-flop maintains a voltage level from a previous time interval.]; and

a comparison circuit for detecting a change in said voltage level from the previous time interval [28-1 – 28-N Fig 2; col. 2 lines 62-65; col. 3 lines 33-61; col. 4 lines 15-20] indicating an assertion of a signal by another device [col. 1 lines 14-17. The logic generating the data signals T1-TN is interpreted to be another device.]

It would have been obvious to one of ordinary skill in the art to combine the teachings of Gulick and Kanuma to incorporate a memory element for maintaining a voltage level and a comparison circuit to use the stored voltage in the memory element in order to detect change in voltage level from one time interval to the next thus indicating a change in power consumption state.

7. As per claims 7 and 15, Gulick does not explicitly teach a high logic applied to an exclusive-OR gate with the voltage level from the previous interval to determine the signal level in the current time interval.

Kanuma teaches the input data applied to an exclusive-OR gate with the voltage level from the previous time interval to determine the signal level on the bus in the current time interval. [28-1 – 28-N Fig 2; col. 3 lines 37-56].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Gulick and Kanuma to determine the signal level to be asserted in the current time interval on the basis of a comparison by an exclusive-OR gate since the comparison of voltage levels is indicative of whether or not a bus is being driven into a certain power consumption state.

8. As per claims 2, 11, and 17, Gulick does not explicitly teach the step of maintaining the voltage level from the previous time interval using a memory element.

Kanuma further teaches the step of maintaining the voltage level from the previous time interval using a memory element. [22-1 – 22-N Fig 2; col. 3 lines 33-61; col. 4 lines 15-20. Based on the cited lines, it is evident that a D Flip-Flop maintains the voltage level of the previous time interval.]

9. As per claim 21, Gulick further teaches the step of transitioning from a first voltage level to a second voltage level [col. 10 lines 19-26].

10. As per claim 22, Gulick does not explicitly teach a device wherein the adjustment circuit is an exclusive-OR gate.

Kanuma further teaches a device wherein the adjustment circuit is an exclusive-OR gate. [20-1 – 20-N Fig 2; col. 3 lines 37-51]

11. As per claim 23, Gulick does not teach a comparison circuit that is an exclusive-OR gate.

Kanuma further teaches a device wherein the comparison circuit is an exclusive-OR gate. [28-1 – 28-N Fig 2; col. 2 lines 62-65; col. 3 lines 33-61;col. 4 lines 15-20].

12.As per claim 19, Gulick and Kanuma do not explicitly teach the bus being on a system-on-chip.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Gulick and Kanuma to implement the bus on a system-on-chip.

13. As per claim 20, Gulick and Kanuma do not explicitly teach the bus being on a printed circuit board .

It would have been obvious to one of ordinary skill in the art to modify the teachings of Gulick and Kanuma to implement the bus on a printed circuit board.

14. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick [US Pat No. 6,601,178] in view of Azarya et al [US Pat No. 5,978,578].

Gulick does not explicitly teach the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval.

Azarya teaches the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval [col. 13 lines 54-56].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Gulick and Azarya to ensure that only a single node connected to the bus can assert a control signal in order to prevent the bus from being driven into an indeterminate state resulting from simultaneous assertion of signals from different nodes connected to the bus.

15. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick [US Pat No. 6,601,178] in view of Kanuma [US Pat No. 4,587,445] as applied to claim 16 above, and further in view of Azarya et al [US Pat No. 5,978,578].

Gulick and Kanuma do not explicitly teach the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval.

Azarya teaches the step of ensuring that only a single node connected to the bus can assert a control signal in a given time interval [col. 13 lines 54-56].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Gulick, Kanuma and Azarya to ensure that only a single node connected to the bus can assert a control signal in order to prevent the bus from being driven into an indeterminate state resulting from simultaneous assertion of signals from different nodes connected to the bus.

16. Claims 4,5,12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick [US Pat No. 6,601,178].

17. As per claims 4 and 12, Gulick does not explicitly teach the bus being on a system-on-chip.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Gulick to implement the bus on a system-on-chip.

18. As per claims 5 and 13, Gulick does not explicitly teach the bus being on a printed circuit board .

It would have been obvious to one skilled in the art to modify the teachings of Gulick to implement the bus on a printed circuit board.

19. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick [US Pat No. 6,601,178] in view of Buch [US Pat No. 5,230,067].

Gulick does not explicitly teach the step of maintaining the control signal value at the voltage level from the previous interval when no node drives the bus.

Buch teaches the step of maintaining the control signal value at the voltage level from the previous time interval when no node drives the bus. [col. 5 lines 64-68; col. 6 lines 1-5]

It would have been obvious to one skilled in the art to combine the teachings of Gulick and Buch in order to avoid a voltage level transition (when no node drives the bus) that would result in increased power dissipation.

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick [US Pat No. 4,587,445] in view of Buch [US Pat No. 5,230,067] as applied to claim 9 above, and further in view of Albrecht et al [US Pat No. 5,281,822].

Gulick and Buch do not explicitly teach a step of compensating for leakage and cross-coupling effects.

Albrecht teaches a field plate that prevents leakage and cross-coupling. [col. 17 lines 37-40; The field plate compensates for leakage and cross-coupling effects.]

It would have been obvious to one skilled in the art to combine the teachings of Gulick, Buch and Albrecht to compensate for leakage and cross-coupling effects.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
June 10,2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100